Amendments to the Specification

Please replace the following paragraph on page 11 with the following amended paragraph:

Fig. 7d shows a sample-and-hold circuit using the exemplary injection-nulling switch of the present invention which describes the first embodiment.

Please replace the following paragraph beginning on page 11 with the following amended paragraph:

Fig. 7a shows a conventional open-loop sample-and-hold circuit. This circuit is often used to demonstrate problems associated with charge injections and to compare the effectiveness of the charge injection compensation circuits. The circuit comprises a sampling switch, a holding capacitor and a buffer. The sampling switch samples the input signal and stores its value in the holding capacitor during the sampling period when the switch is closed. The actual output is taken from the buffer at the end of the holding period when the switch is turned off. Hence, error voltage would appear during the output period as the turning-off switch injects redundant charges into the high impedance node of the buffer. To compare the compensation effectiveness of the injection-nulling switch, three circuits are simulated with input signals set to 2.7V, a holding capacitor of about 1 pF and a sampling switch using an ideal switch (Fig. 7a), a dummy switch (Fig. 7b) and the exemplary injection-nulling switch (Fig. 7d) of the present invention which describes the first embodiment. The terminal H in the dummy switch or in the injection-nulling switch is connected to the high impedance node of the circuit, which is the input of the buffer. Terminal L, on the other hand, is connected to the input signal. Each of the switch elements (S1 and S2) for the injection-nulling switch is implemented using a single NMOS. The clocks T and Tn, as illustrated in Fig. 5, are performed by T2 and T2db (Fig. 7d) in the circuit, respectively. One end of the capacitor C

(value of about 1pF) that is connected to a reference voltage is tied to the analog ground. These connections are maintained for each of the embodiments described below, and are used for exemplary purposes. Fig. 8 illustrates the simulation results of the three described circuits. It can be seen that during the nulling phase (T2db on), the redundant charges injected previously by turning off the switch S1 (T2 off) are nulled by the action of turning on the switch S2 (T2db on) and absorbing them into the capacitor (comparing the curve of the ideal switch). As for the dummy switch, the charge injection remains. The inaccuracy (15nV) of the output is caused by the offset of the buffer. The percentage error caused by the switches are indicated in the plots by 'DS Error' and 'INS Error' where 'DS Error' means percentage error caused by the dummy switch and 'INS Error' indicates the percentage error due to injection-nulling switch.